



Vrije Universiteit Brussel

Design and Analysis of an On-Chip Programmable Op-Amp based Filter

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Promotor Prof. Dr. ir. Gerd Vandersteen



electronic SYStem IDentification test-bench

Programmable chip to simulate a wide class of systems.

- Experimental verification of system identification techniques
- Useful for labs on system identification

electronic **SY**Stem **ID**entification test-bench

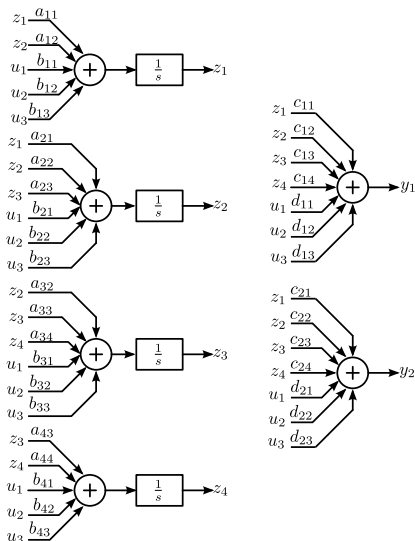
Programmable chip to simulate a wide class of systems.

- Experimental verification of system identification techniques
- Useful for labs on system identification
 - High-level architecture
 - Op-amp design
 - Nonlinear analysis

Architecture

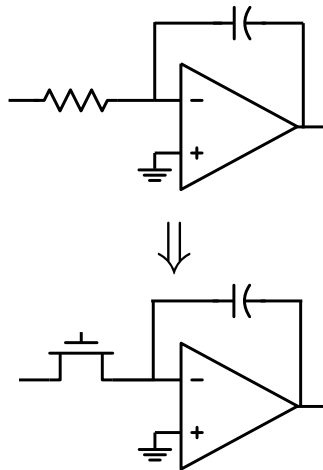
State-Space

$$\begin{cases} \dot{\mathbf{x}}(t) = \mathbf{A}(p, q)\mathbf{x}(t) + \mathbf{B}(p, q)\mathbf{u}(t) \\ \mathbf{y}(t) = \mathbf{C}(p, q)\mathbf{x}(t) + \mathbf{D}(p, q)\mathbf{u}(t) \end{cases}$$



MOSFET-C

- Continuous time filter
- Low bandwidth
- High SNDR
- Better tune-ability than RC integrators

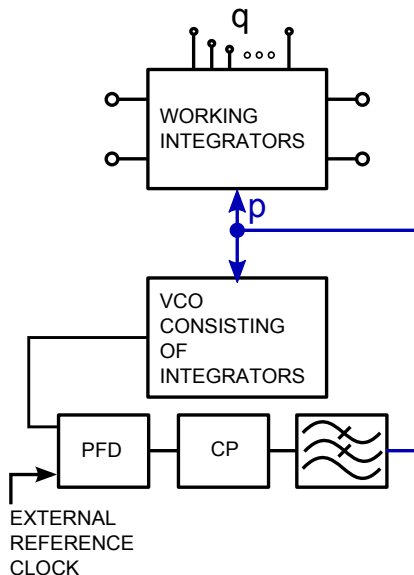


Tuning scheme

PLL-based tuning network

- Build VCO with two integrators
- Set oscillation frequency to precisely known external reference

⇒ High precision + repeatability



Op-Amp

Op-amp is critical to the performance of the MOSFET-C integrator

- High gain needed: $\pm 80\text{dB}$
- *GBW* of about 100MHz
- load capacitance C_L of 10pF.

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-
- 2 stage op-amp
 - Miller compensation
 - Ahuja compensation
 - Fully Differential op-amp
 - Final Design

Design Plan Sansen

Two equations

$$GBW = \frac{g_{m1}}{2\pi C_C}$$

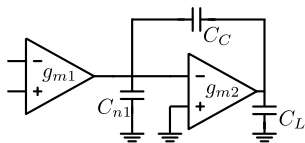
$$f_{nd} = \frac{g_{m2}}{2\pi C_L(1 + C_{n,1}/C_C)}$$

Design parameters:

$$\alpha = C_L/C_C = 3$$

$$\beta = C_C/C_{n1} = 3$$

$$\gamma = f_{nd}/GBW = 3$$



Ahuja Compensation

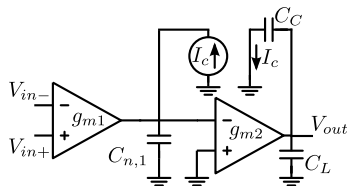
Improvement over Miller compensated op-amp

- RHP zero compensation
- Lower current consumption

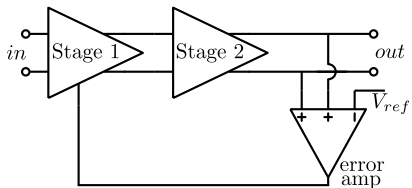
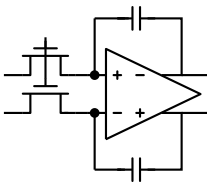
$$GBW = \frac{g_{m1}}{2\pi C_C}$$

$$f_{nd} = \frac{g_{m2}}{2\pi(C_C + C_L)} \frac{C_C}{C_{n1}}$$

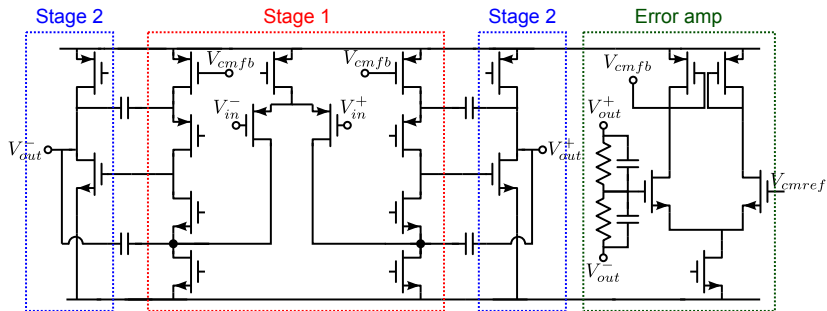
Design plan can be recycled



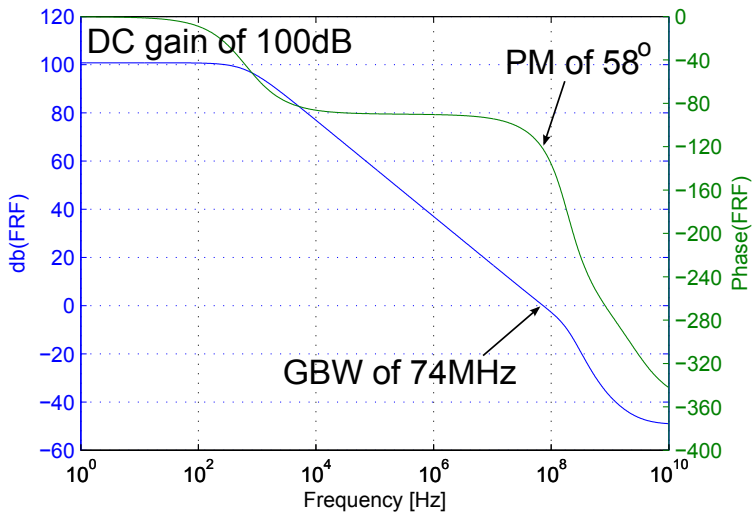
Fully Differential



Design results



Design results



Nonlinear Analysis

We have the op-amp, How to improve its performance?

- Noise performance → Noise analysis
- Nonlinear performance → ???

Nonlinear Analysis

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Nonlinear Analysis

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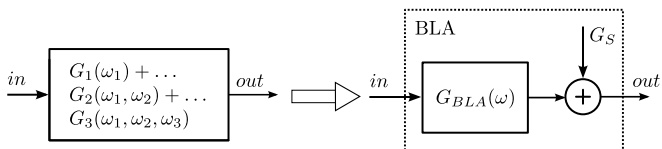
- Noise performance → Noise analysis
- Nonlinear performance → **Nonlinear analysis**

Overview

- Method
 - Single-ended op-amp
 - Fully differential op-amp
- } Published in conference paper

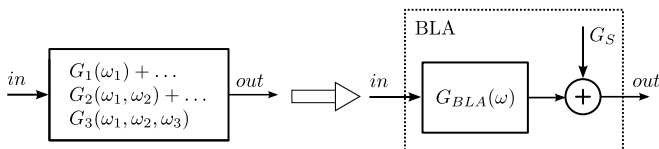
Idea Behind the Analysis

■ Best Linear Approximation



Idea Behind the Analysis

■ Best Linear Approximation

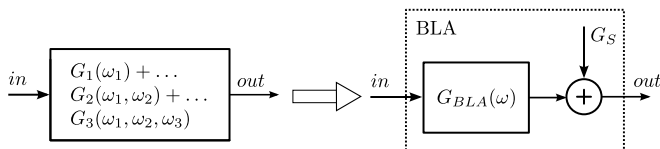


■ Spectral Correction

$$G_S(\omega) = out(\omega) - in(\omega) \cdot G_{BLA}(\omega)$$

Idea Behind the Analysis

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■ Spectral Correction

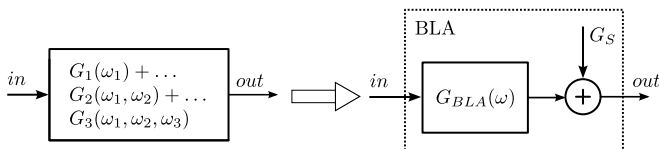
$$G_S(\omega) = out(\omega) - in(\omega) \cdot G_{BLA}(\omega)$$

■ Assume linearity

$$G_{BLA} = ACFRF$$

Idea Behind the Analysis

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$$G_S(\omega) = out(\omega) - in(\omega) \cdot G_{BLA}(\omega)$$

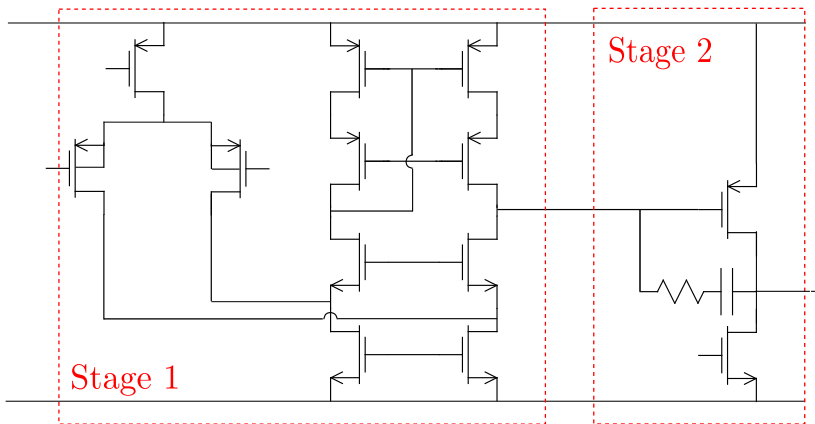
■ Assume linearity

$$G_{BLA} = ACFRF$$

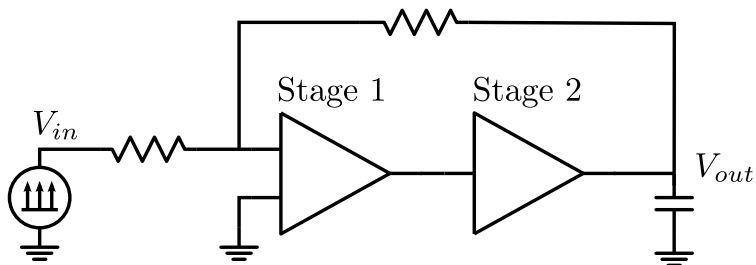
■ Noise Analysis

Refer nonlinear contributions to the output to compare them

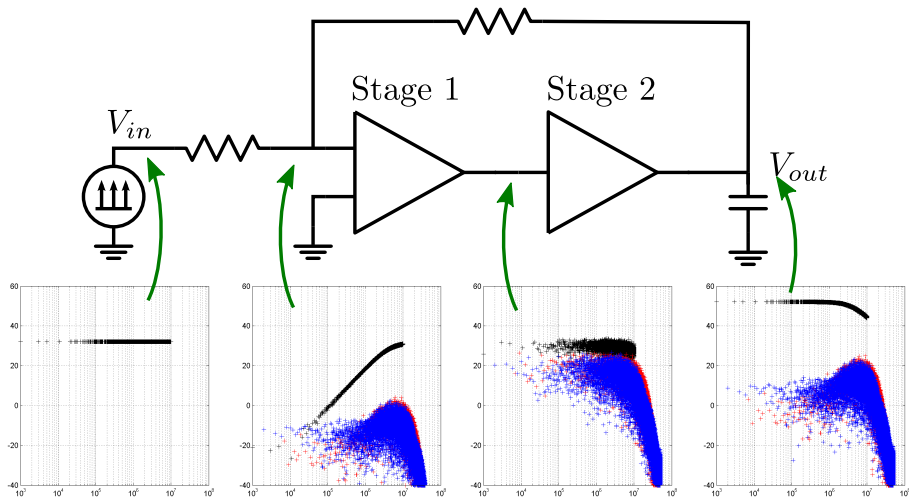
Single-Ended Op-Amp



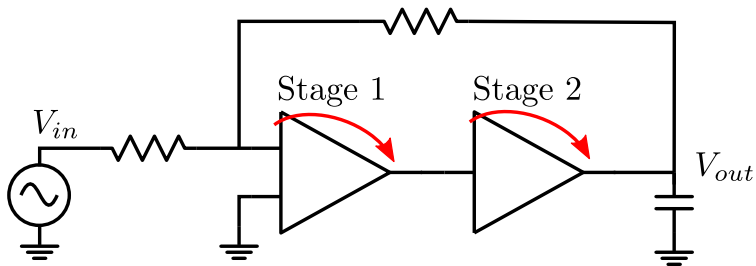
Step 1: Transient Analysis



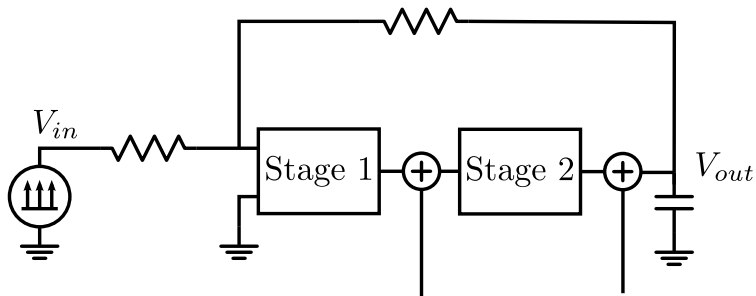
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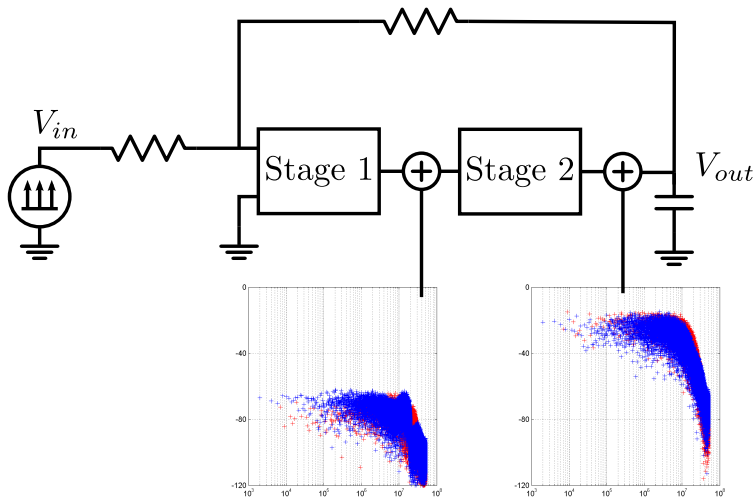
Step 2: Spectral correction



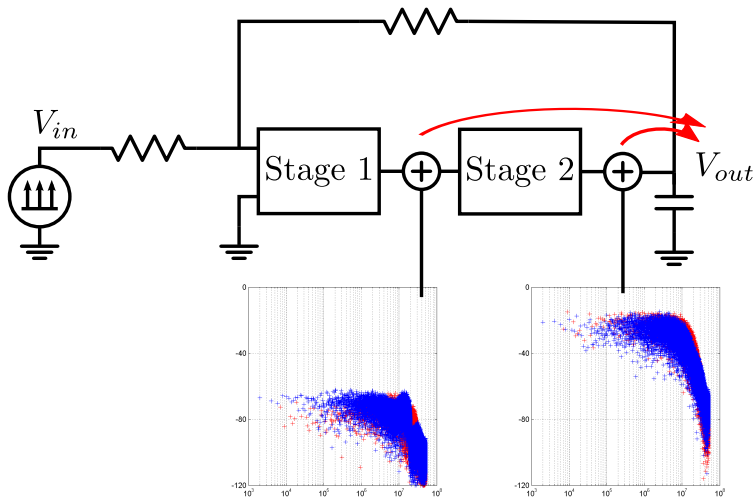
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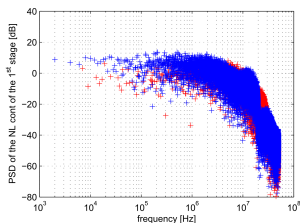


Step 3: Refer to the output

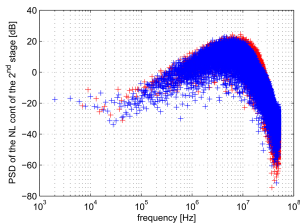


Results

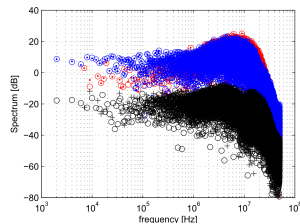
Stage 1 at output



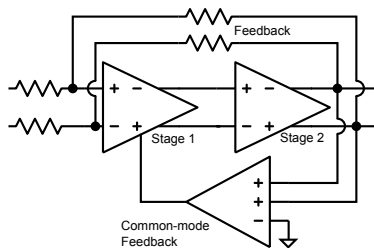
Stage 2 at output



Sum of contributions vs simulated output



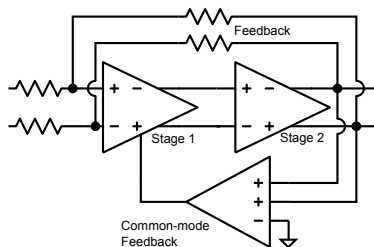
Extension to Fully-Differential Op-Amps



The method remains the same, but:

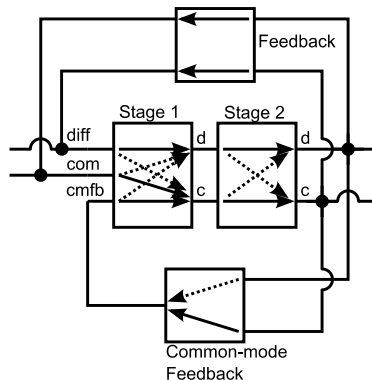
- MIMO
- Differential and Common mode
- Extra stage (Error amp)
- Assume symmetry

Extension to Fully-Differential Op-Amps



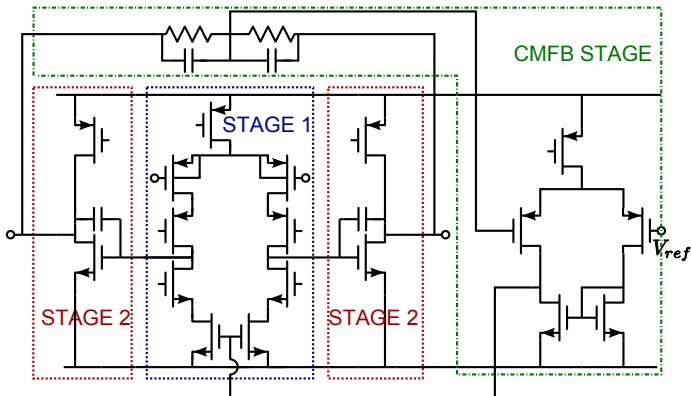
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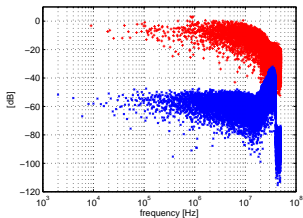
—————> Dominant
> Negligible

Fully-Differential Op-Amp under test

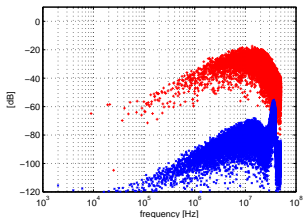


Results Differential Analysis

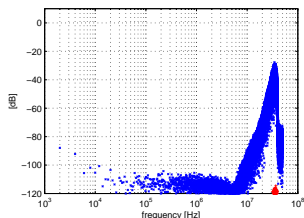
stage 1 at output



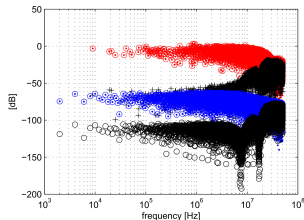
stage 2 at output



CMFB stage at out



error made on the differential mode



Future Research

- Simplify analysis
- Quicken analysis
- Improve accuracy

Overview

- System-Level architecture
- Op-Amp Design
- Nonlinear Analysis

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Continue the design of the chip

- Improve nonlinear performance of the op-amp
- Apply nonlinear analysis to complete architecture

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- System-Level architecture
- Op-Amp Design
- Nonlinear Analysis

Continue the design of the chip

- Improve nonlinear performance of the op-amp
- Apply nonlinear analysis to complete architecture
- Design of the tuning network
- ESD, Yield, Lay-out