Project High-Frequency Electronics

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***Abstract*—The goal of the project for High-frequency electronics is to design and build an amplifier for frequencies around 3GHz. You will learn to work with S-parameters, design matching networks and biasing networks, verify the stability of the amplifier and lay-out your design. Finally, you will solder the circuit and measure its performance on a vector network analyser.**

All amplifier designs start by choosing the operating point for the transistors involved in the circuit. You will be using the BFP520 bipolar transistor of infineon in your amplfier. Performing a thorough DC analysis of the BFP520 bipolar transistor is imperative to obtain a good result in the end (Section I). For the obtained DC operating point, you will determine the S-parameters of the transistor (Section II), these S-parameters will allow you to design a matching network at the desired frequency using ideal transmission lines (Section III). The amplifier will be built with microstrip lines, so you will have to translate your ideal matching network into a microstrip network (Section III-C). Then you will design a DC biasing network and ensure it does not influence the behaviour of the amplifier at high frequencies (Section IV). Once you obtain both the bias network and the matching network, you have to ensure the amplifier is stable at all frequencies (Section V). Finally, you lay-out the circuit and build it, such that its real performance can be measured on the Vector Network Analyser (Section VI).

We will use Keysight's Advanced Design System (ADS) to simulate and design the circuit. A short introduction into ADS is included at the end of this document.

I. DC ANALYSIS

The first step of the design is to determine the DC operating point of the BJT. The DC operating point determines the final performance of the amplifier. High collector currents give higher gain, but result in a larger power dissipation and higher noise, while low power dissipation usually leads to stability problems and lower gain. The curves that predict the gain and noise for the BFP520 in function of the operating point are shown in Figure 1.

You will be given an operating point for this assignment. We specify the collector current (I_c) and collector voltage (V_c) to use during the design of the amplifier, what remains is to determine the corresponding base voltage (V_b) and base current (I_b) of the transistor using ADS simulations. Use a voltage source to set the collector voltage and sweep the base current with a DC current source in DC simulations in ADS. Sweep until you obtain the correct collector current. We included the datasheet of the transistor at the end of this document. Note that the datasheet specifies a typical h_{FE} of 110 for the BFP520.

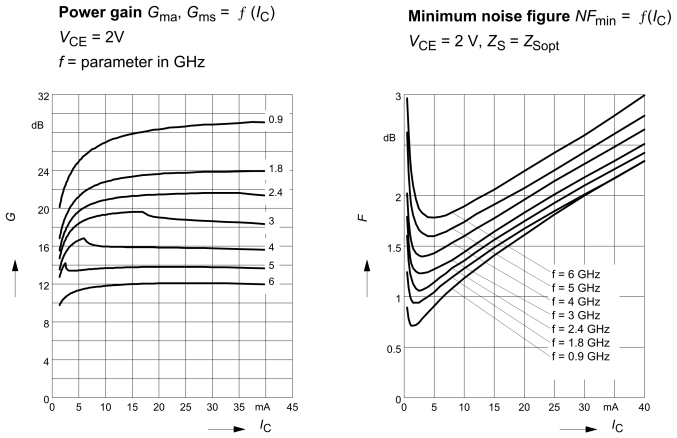


Figure 1. The choice of DC bias point is very important for the performance of the amplifier. It influences the gain, stability, power consumption and noise of the final design. This figure shows curves of the BFP520 that show the noise and gain of the transistor in function of its collector current.

II. DETERMINE THE S-PARAMETERS

Now that you know the required base voltage and collector voltage, you can determine the small-signal behaviour of the transistor around the operating point. The S-parameters of the transistor provide the complete picture of the small-signal performance of the transistor at the design frequency. The S-parameters relate the incident waves at the ports of the transistor to the reflected waves at the same ports.

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix}$$

$$S_{11} = \left.\frac{b_1}{a_1}\right|_{a_2=0} \quad \text{Input reflection coefficient}$$
$$S_{21} = \left.\frac{b_2}{a_1}\right|_{a_2=0} \quad \text{Forward gain}$$
$$S_{12} = \left.\frac{b_1}{a_2}\right|_{a_1=0} \quad \text{Reverse gain}$$
$$S_{22} = \left.\frac{b_2}{a_2}\right|_{a_1=0} \quad \text{Output reflection coefficient}$$

More details about the definition of the S-parameters can be found in the theoretical part of the course.

Determining the S-parameters in ADS is done with an S-parameter simulation. In ADS, the *Term* component is used to indicate a port, the characteristic impedance of that port and its number. The simulation returns the S-matrix between these *Term* components at the specified frequencies.

To avoid disturbing the operating point with the 50Ωresistors inside the Term components, use ideal coils and capacitors to block AC and DC signals respectively. An example of

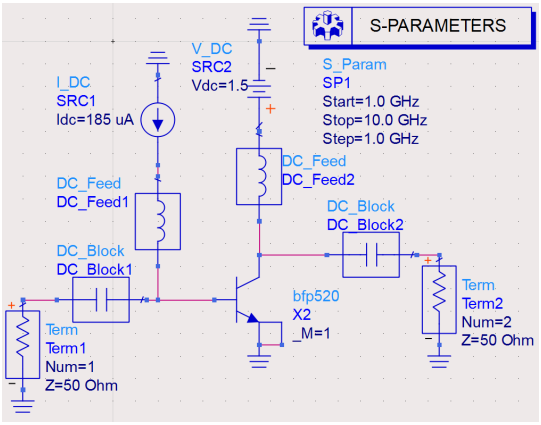


Figure 2. Simulation set-up used to determine the S-parameters of the transistor.

the simulation set-up needed to determine the S-parameters is shown in Figure 2.

III. Design the matching network

Now that you know the S-parameters of the transistor, you can start designing its matching network. A matching network is a (passive) network that transforms the terminal impedances (50Ω) into reflection factors preferred by the transistor. Usually, two matching networks are used: one at the input and one at the output (Figure 3). The matching network at the input creates Γ_s at the transistor input. The output matching network creates Γ_l at the collector of the transistor. The wanted values for Γ_s and Γ_l depend on the S-parameters of the transistor and on specific requirements for the amplifier:

- For high gain, a conjugate match is the optimal solution. In a conjugate match, the reflection factors seen from the transistor are equal to the complex conjugate of the reflection factor presented by the transistor: $\Gamma_{in} = \Gamma_s^*$ and $\Gamma_{out} = \Gamma_l^*$
- In a Low-Noise Amplifier the reflection factor seen at the input of the transistor Γ_s is set to the reflection factor that gives the lowest noise. Classically this reflection factor is called Γ_{opt}. At the output, a conjugate match is presented. $\Gamma_{out} = \Gamma_l^*$.
- To obtain a high output power, a low impedance is presented to the output of the transistor. This limits the voltage swing at the drain for the high currents provided by the transistor.

The course notes go into great detail how to make trade-offs between gain, stability and noise by playing with the reflection factors. Other good references include [1] and [2].

A. Matching a unilateral device

To simplify the matching process, start by assuming the device is unilateral. This means that there is no reverse gain in the transistor ($S_{12} = 0$). In this simplified case, the reflection factor seen at the input of the transistor:Γ_{in} does not depend on the reflection factor presented at the output of the device Γ_l.

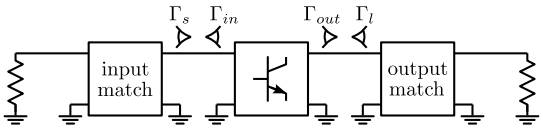


Figure 3. Matching of a transistor consists of adding an input and output matching network that transform the terminal impedances into the wanted Γ_l and Γ_s

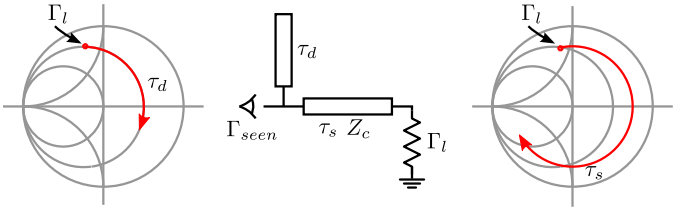


Figure 4. Effect of a delay line and a stub on the reflection factor. The delay line rotates the reflection factor around the point corresponding to its characteristic impedance. The stub only modifies the imaginary part of the impedance, so it follows an impedance circle with a constant real part.

Also, the reflection presented at the collector of the transistor Γ_{out} is independent of Γ_s which makes matching easy. If $S_{12} = 0$, then $\Gamma_{in} = S_{11}$ and $\Gamma_{out} = S_{22}$. Performing a conjugate match then just boils down to synthesising the complex conjugate of S_{11} and S_{22} with the input and output matching networks respectively. You can use an *S2P_eqn* bock in ADS to represent the unilateral device and design your matching network to obtain a conjugate match for this simplified situation.

Many different topologies can be used to build the matching network and you can try several of them if you want. A classic solution is to match the transistor with a single-stub matching network shown in Figure 4. By playing around with the time-delay τ and the characteristic impedance Z_c of the transmission lines, a load reflection Γ_l can be transformed into a wanted reflection factor Γ_{seen}. You can refer to your notes from third bachelor or to [1] for the details on the calculations involved in stub matching. Start by using ideal transmission lines *TLIN* and *TLOC* in your matching network. We will replace the ideal lines by real microstrip lines in a later step of the design. To help you during the matching, you can use *SP_probe* components to determine the different reflection factors around the transistor while tuning the length of the different lines in the matching network.

B. Matching a bilateral transistor

When you matched the unilateral device, you can move to the more general case, where $S_{12} \neq 0$. A device with a non-zero reverse gain S_{12} is called bilateral. All devices show some reverse gain, which should be taken into account during the matching. In the theoretical part of the course, two important expressions were obtained for the reflection factors in the circuit of Figure 3:

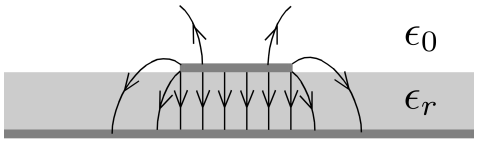


Figure 5. A cross section of a microstrip line

$$\Gamma_{in} = S_{11} + \frac{S_{21}\Gamma_l S_{12}}{1 - S_{22}\Gamma_l}$$
$$\Gamma_{out} = S_{22} + \frac{S_{21}\Gamma_g S_{12}}{1 - S_{11}\Gamma_g}$$

Obtaining a conjugate match at both input and output requires $\Gamma_{in} = \Gamma_g^*$ and $\Gamma_{out} = \Gamma_l^*$. The expressions now show that Γ_{in} depends on the matching network at the output through Γ_l. Matching the output will break the match at the input, because the reflection factor changes.

Usually, the reverse gain is very small, so the match obtained in the assumed unilateral case is very good. A few more iterations of matching the input and output will bring you to the optimum in the bilateral case. Perfectionists can solve the set presented by the using the *SmGamma* block in ADS. This simulation components returns the required Γ_l and Γ_g needed for a simultaneous conjugate match at both input and output.

C. Matching with microstrip lines

By now, you should have a transistor with a matching network that consists of ideal transmission lines. Ideal transmission lines are quite rare in real life, so we have to find a way to realise the wanted characteristic impedance and delays. Many different technologies exist[1], but for this project, microstrip lines will be used.

A microstrip line is a PCB trace with a ground plane below it. Figure 5 shows such a microstrip line. The characteristic impedance of the line is determined by the width of the line. Its delay is determined by the length. ADS has a built-in tool to design microstrip lines which is called LineCalc. This small tool requires the information of the substrate, the operating frequency and the desired transmission line parameters to calculate the width and length of the corresponding microstrip line.

We use a Rogers 4360 substrate with a thickness of 40mil. This substrate is especially designed for high frequencies with a very controlled dielectric constant and low losses at these high frequencies. Cheaper materials, like the commonly used FR4, can introduce high losses and are usually not suited for these high-frequency applications. The datasheet with all the material properties of the Ro4360 PCB is included at the end of this document.

You can start up the LineCalc tool by going to a schematic window and by pressing *Tools→LineCalc*. The interface of

[1]On a PCB, the options include: stripline, coplanar waveguide, slotline, microstrip lines, ... Other options include waveguides and even coaxial cables

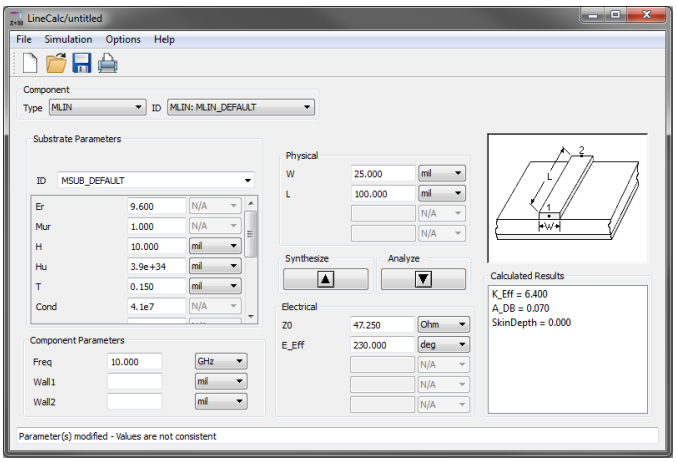


Figure 6. The LineCalc tool can be used to determine the parameters of your microstrip lines.

LineCalc is very intuitive (Figure 6). The PCB information and the operating frequency are required on the left, while the microstrip line information is entered on the right. You can specify the characteristic impedance and the wanted electrical length on the bottom right and then click the *Synthesise* arrow to obtain its corresponding width and length of the microstrip line. Ensure that the dimensions of the result are set to mm first, before synthesising your line.

IV. Design of the biasing network

The design of the biasing network often makes or breaks the working of the amplifier in its application. The biasing network fixes the DC operating point of the transistor, but should not influence the behaviour at RF frequencies. Additionally, the bias network should ensure temperature stability of the operating point and ensure stability of the whole amplifier. The design of the biasing network consists of three steps. In the fist step, a resistor network is designed around the transistor to bring it in its in the correct operating point and guarantee temperature stability of this operating point. In the second step, the biasing network is modified to ensure it does not influence the RF behaviour of the circuit. In a third step, the biasing network is adapted to ensure stability of the amplifier at all frequencies.

A. DC biasing

The operating point of the transistor is set by specifying its collector current I_c and its collector voltage V_c. When the supply voltage is known, the collector resistor be determined easily. The BFP520 cannot handle voltages above $2.5V$, so this is the maximum supply voltage you can use. Otherwise you risk damaging the transistor in operation. The main difficulty in the design of the bias network lies in providing the correct voltage to the base of the transistor. Several options are shown in Figure 7.

The first two biasing networks (Fig. 7a and b) can work, but they rely on transistor parameters to fix the operating point.

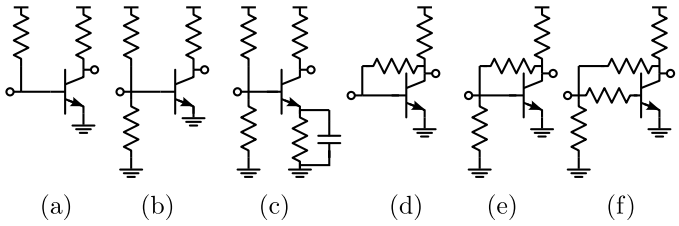


Figure 7. Different biasing networks for the bipolar amplifier. (a) and (b) are basic biasing networks without feedback (c) shows emitter degeneration (d) (e) and (f) are biasing networks with a grounded emitter lead.

This is bad practice, because the transistor parameters change with temperature. Using feedback, we can make it such that the operating point only depends on resistor values, which are a lot more stable.

In designs for low frequencies, emitter degeneration is commonly used (Figure 7c). Emitter degeneration has the drawback that the gain of the transistor drops, but this can be overcome by introducing a capacitor in parallel with the emitter resistor. Adding all these elements at the emitter is not good for stability however. RF transistors usually want the emitter to be grounded with the lowest parasitic inductance at their emitter (this is why the transistor has two emitter leads on its package). Adding extra parasitic inductance by applying emitter degeneration is a very bad idea then.

Figure 7(d) (e) and (f) show biasing networks with feedback and a grounded emitter lead. Voltage feedback is applied from collector to base. If the collector current rises, the voltage at the collector goes down. With it, the base voltage goes down as well, so the collector current will decrease. Several options still exist, each with certain benefits [3]

(d) Doesn't allow a lot of design freedom, but is very robust against temperature variations. It is not very robust against process variations or model errors however.
(e) Adding an extra resistor fixes the base voltage. This makes the bias network robust against model errors, but is becomes more sensitive to temperature variations
(f) Adding a large resistor to the base fixes the base current and makes the network more robust against temperature again.

It's up to you to choose the appropriate bias network, experiment with several ones, or maybe even consider an active bias network. Note that the choice of biasing network is also influenced by the stability of the amplifier (Section V). Some biasing networks are more flexible to add the changes required to ensure stability at all frequencies.

B. Making the biasing network invisible at RF

Now that you have chosen a bias network, you should guarantee that it doesn't influence the performance of the amplifier at RF frequencies. This goal is obtained by making sure the bias network presents itself as an open circuit at the RF frequencies. Placing the bias network in parallel with the matching network then ensures that both do not influence each-other.

An easy way to avoid influence from the bias network at RF frequencies is to use large-valued capacitors and inductors. Large capacitors acts as short circuits for the high frequencies, so they can be used to block the DC signal, but allow the RF signal to pass through. Large valued inductors block RF signals, but allow DC to pass through, so they can be used in the path from the bias network to the transistor.

Figure 8 shows the classic way coils and capacitors are used at the base of a transistor. This circuit is called a Bias Tee. The RF signal can reach the base and is bocked by the coil, so it cannot flow into the bias network. The DC current can flow through the coil into the base, but is blocked by the capacitor, to prevent the DC current to flow into the 50Ω termination added to the RF input.

Building a bias tee at very high frequencies with coils and capacitors can be difficult due to the parasitics in the used elements. Parasitic capacitance between the windings of an inductor will create a resonant tank in the inductor with an associated Self Resonance Frequency (SRF). Figure 8 shows the typical behaviour of an inductor for high frequencies. Around the SRF, the inductance value changes heavily. A capacitor shows similar behaviour. We attached the datasheet of a high-frequency $5.6\mathrm{pF}$ capacitor that you can use in your design at the end of this document.

The message here is that the impedance value of the elements cannot be trusted around the SRF. Applications that require a controlled impedance (like filters and matching networks) use components with a SRF which is 10 times higher than the operating frequency [4]. The higher the inductance value, the lower the SRF, this limits the available range of inductors that can be used in a certain application. When components get smaller, the SRF goes up, to very high frequency applications tend to use tiny surface mount components, for their good high-frequency performance.

One can note that the inductor behaves almost as a perfect open at its SRF. Capacitors behave close to the perfect short around their SRF. In bias networks, where the actual value of the impedance is not so very important, working at the SRF of the components is a good thing. Precise control over the SRF is hard to obtain however, because it depends on the PCB properties, the amount of traces around the element and on process variation inside the inductor/capacitor. The SRF specified by the manufacturer (if they specify it at all) is only an indicative value.

An alternative to the bias tee with lumped elements, which doesn't require an expensive inductor, is to use a $\lambda/4$ line with a capacitor to obtain an open at the operating frequency (Figure 8). The capacitor creates a short to ground at high frequencies, which is changed into an open by the transmission line with length $\lambda/4$. The inductor is added for a little extra protection, but examples 1 and 2 show that it is not really required. The designers there even remove the capacitor to ground an replace it with large metal islands on the PCB, which can act as a short. One can also add another $\lambda/4$ line, terminated in an open to the circuit to provide an even better short, as is done at the input of example 1.

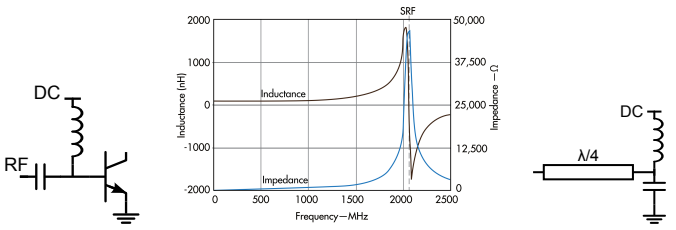


Figure 8. To avoid influence of the bias network at RF, a bias tee is added to the circuit. A classic implementation is shown on the left. Capacitors and inductors can show unusual behaviour at high frequencies though, due to their self-resonance (shown in the middle [4]). Constructing a bias network with a $\lambda/4$ line can be a good alternative when the right coils and capacitors are not available.

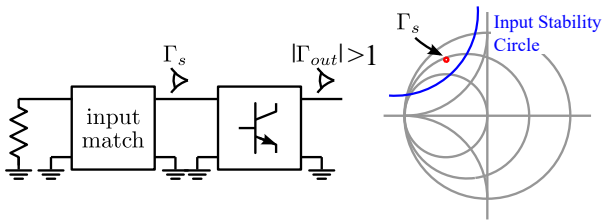


Figure 9. This unstable circuit has an output reflection factor $|\Gamma_{out}| > 1$. This can be confirmed by the fact that the reflection factor presented by the input matching network lies on the wrong side of the input stability circle of the transistor.

V. Check the stability

An amplifier should be stable at all frequencies. During the design of high-frequency amplifiers, it happens that unwanted oscillations are observed in the final amplifiers. Often, these oscillations occur outside of the band of interest, but they cannot be ignored! An oscillating transistor is pushed hard into compression and this will influence the performance of the amplifier in the band of interest.

Stability of basic high-frequency circuits has been studied in the theoretical part of the course and is also detailed in [1] and [5]. The results can be summarised into two basic rules. A circuit is unconditionally stable if

1) The poles of the two-port network under investigation with ideal terminations (open or short circuit) all lie in the left half plane
2) μ is larger than 1

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \det(\mathbf{S})| + |S_{21}S_{12}|}$$

The first condition is very hard to verify and requires either access to the internal nodes of the active device or good software to estimate the location of the poles of the amplifier. Verifying the second condition can be done in ADS using a measurement expression. For this project, you should only consider the condition on μ, keeping in mind that you can be fooled by the circuit if the first condition is not satisfied.

Probably you will encounter certain frequencies where the circuit is not unconditionally stable $\mu > 1$. At these critical frequencies you can use the stability circles to determine the zone of load impedances that yield a stable circuit. For example, the input stability circle specifies the load reflection factors Γ_l for which the norm of the reflection factor seen at the input of the device becomes unity ($|\Gamma_{in}| = 1$). An example of this is shown in Figure 9.

You can use *SP_probes* to determine the reflection factors seen from the transistor (Γ_s and Γ_l) and use the stability circles of the transistor at the right frequency to find out whether the stability issue is due to the input or the output matching network. Then you should adapt your matching and bias network to solve the stability issues without influencing the performance of the matching or biasing networks too much. This can be a tricky task. Some options you can consider are:

- Avoid working with very long transmission lines in the matching network, they will make the reflection factor move a lot in function of frequency, complicating the solution of the problem
- Problems at low frequencies can be solved by changing the resistance values in the bias network, or adding an RC circuit to ground, as is done at the base of example 3
- Modifying the capacitor and inductor values in the bias tee
- Reducing the gain, by adding series resistance in the matching network

VI. Generate the lay-out

When the circuit is matched, biased correctly and stable for all frequencies, you can start to generate the lay-out. ADS can generate the lay-out of a schematic automatically by clicking *Layout→Generate/update*. Your first lay-out will probably not look like nice yet. You'll have to perform the following steps to ensure ADS can generate the lay-out correctly:

- Add *MTEE* and *MCROSO* components on the interconnections between transmission lines and stubs.
- All resistors, inductors and capacitors will have to be replaced by their corresponding components with the correct footprint (*R_PAD*, *L_PAD* and *C_PAD*). We have 0805 surface mount components available in our lab, so use the correct footprint size for those components
- Passive components don't come in any value. You'll have to adapt the values of your passives to make sure we have the components available in the lab, or use series and parallel connections of existing components to get that specific resistor value you want
- Make sure all ground connections are provided using *VIAGND*. Vias introduce parasitic inductance, so use multiple vias for critical ground connections.
- Add extra 50Ωtransmission lines at the input and output of your circuit to provide room for the SMA connectors. The datasheet and recommended footprint for the available SMA connector is attached to the end of this document.

A list of useful components for the lay-out is provided at the end of the document. If you use all correct components in your schematic, the complete lay-out of the circuit can be generated automatically.

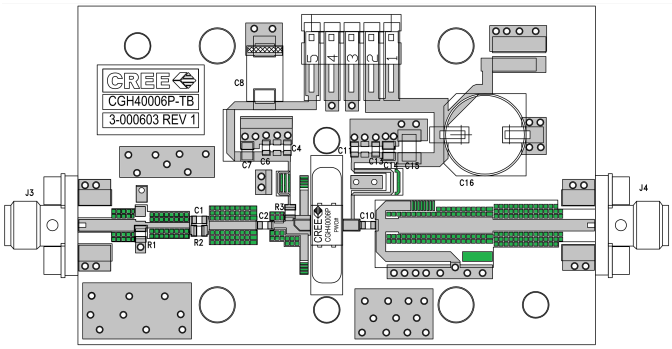


Figure 10. Professional designs for testing add "chicken dots" to the circuit. These provide a way to manually increase the length of stubs to change the matching network slightly. The chicken dots are shown in green on the design of a Cree power amplifier test board.

Extra lay-out options to consider

- Take into account that your PCB will be manufactured with a milling machine. The finest drill in the milling machine has a diameter of 10mil (0.25mm), so that gives the smallest possible distance between two metal traces. Also traces with a width smaller than 15mil (0.4mm) cannot be fabricated reliably.
- Give all your Vias the same diameter to avoid too much work for our technician Johan. I usually use a VIA diameter of 0.8mm, because it is the diameter of a common wire in the lab, which then fits easily.
- Leave some room for extra components in the biasing networks. Maybe extra decoupling capacitors or stabilising resistors are required. It would be a shame if you don't have room for those.
- Consider adding chicken dots, for the fine-tuning of your matching network (Figure 10). But do make sure they don't influence the circuit.
- Use the top metal to annotate important messages on your PCB, like the supply voltage, maybe even specify the operating point and the frequency somewhere.
- You can set-up an electromagnetic co-simulation of your final lay-out to determine the circuit behaviour more accurately. This momentum simulation allows to take coupling between different lines into account.

VII. Build the circuit

When the lay-out is finished, check whether everything still works by performing your final simulations. Then you can prepare to generate the Gerber files. First add the board outline to your lay-out on an unused layer. This rectangle indicates where your PCB ends and can be cut. Make sure to leave at least 1mm extra room around your circuit to cope with errors on the cutting of the PCB. Also, ensure enough room is left around each transmission line and stub.

If you have added the board outline and done the final checks of your design you can generate the Gerber files for processing. Click *File→Export* from the lay-out window and make sure you export all the necessary layers. Usually these are *Cond1*, *Drill/Hole* and the layer of the board outline. The generated Gerber files are placed in your workspace folder under "mfg". You can check whether they are correct by uploading them to www.circuitpeople.com.

The milling of the PCB is done by Johan Pattyn. You can e-mail your Gerber files to him (Johan.Pattyn@vub.ac.be) to have your circuit made. Johan has a lot of work, so keep in mind that it can take over a week to make your PCB. When you receive the PCB, you can solder the components on.

VIII. Measure the performance

When you soldered all the components to the PCB, you are almost ready to measure the actual performance of your amplifier. First, check whether the biasing of the transistor is correct: Apply the supply voltage and measure the resulting collector current and voltage. To prevent your circuit from oscillating, screw 50Ω terminations to the input and the output of your amplifier while testing the bias. Then you can make an appointment with Adam, Maral or Yves to measure the performance of your circuit. We will measure the S-parameters of your total circuit together on a Vector Network Analyser (VNA). Bring a USB drive, so that you can save the measurements and compare them to the simulation results later on.

References

[1] G. Gonzalez, Microwave Transistor Amplifiers. Analysis and Design. Prentice Hall, 1996.
[2] E. Fooks and R. Zakarevicius, Microwave Engineering Using Microstrip Circuits. Prentice Hall, 1990.
[3] "Application note 1293: A comparison of various bipolar transistor biasing circuits," Avago Technologies, Tech. Rep., 2010.
[4] "Investigating inductor requirements for power and rf/microwave designs," Coilcraft, Tech. Rep., 2014.
[5] R. Jackson, "Rollett proviso in the stability of linear microwave circuits-a tutorial," Microwave Theory and Techniques, IEEE Transactions on, vol. 54, no. 3, pp. 993–1000, March 2006.

IX. Some more random suggestions

- Save all your files on the Z:\ drive on your computer. This network drive can be accessed from all ELEC computers.
- Make sure there are no spaces in the path to your workspace, it can cause weird errors while simulating.
- Pay very close attention to the warnings given by the simulator, they can indicate errors you made in the design of the circuit.
- Always check the operating point of the transistor when something goes wrong. You can visualise DC voltages and currents by clicking *Simulate→Annotate DC solution.*

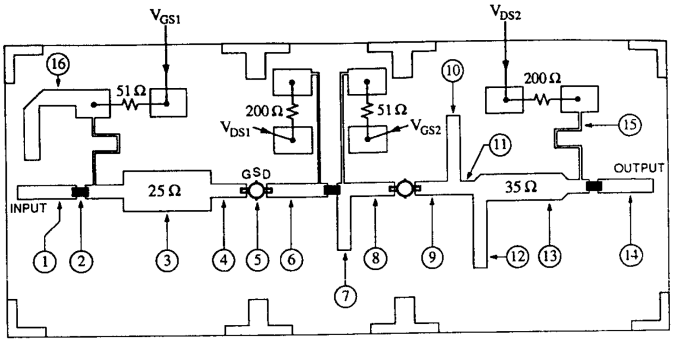


Figure 11. First example of a two-stage LNA (from [2]).

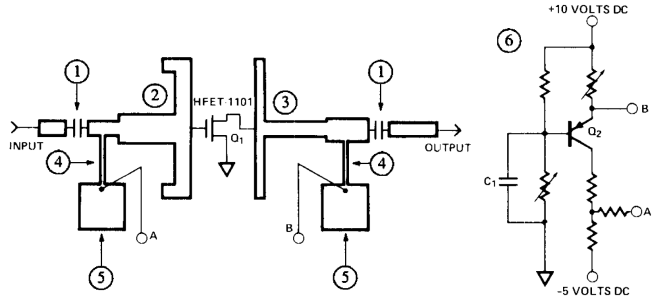


Figure 12. The second example of a 6GHz amplifier (modified from [1])

APPENDIX

Here, we show some selected examples of high-frequency amplifiers extracted from literature, which are similar to the circuit you will design. You can use them as inspiration for your own design.

A. *Example 1:* 6GHz *Low-noise amplifier*

The first example comes from [2] and is shown in Figure 11. The circuit is a 2-stage LNA consisting of GaAs FETs. (1) and (14) are 50Ω lines for connections to the coaxial cables. (2) is a DC blocking capacitor. The matching network consisting of (3) and (4) provide the optimum low-noise reflection coefficient to FET (5). The FETs are both placed in a common-source configuration. The matching network consisting of (6) (7) and (8) transforms the output impedance of the first FET into the optimum low-noise reflection coefficient for the second FET. Finally, (9) (10) (11) (12) and (13) provide a conjugate match at the output of the second FET. The biasing is done through high-impedant $\lambda/4$ lines (15). The short at the end is created by the big pads where the bias resistors are connected. An even lower impedance is provided at the input by the open-circuited $\lambda/4$ line (16).

B. *Example 2:* 6GHz *amplifier from Hewlett-Packard*

The second example originates from an application note of Hewlett-Packard. A detailed description about this design can be found in [1]. (1) are DC blocking capacitors. (2) and (3) are the input and output matching network respectively. The designers use quarter-wave impedance transformers in the matching network, instead of a classic single-stub match. Note that the stubs are placed on both sides of the matching network. This is done to minimise transition interactions between the impedance transformers and the stubs. (4) and (5) create the biasing network. Both are $\lambda/4$ lines, The first one is a high-impedant line going to the circuit, while (5) is made large to provide a big capacitance to ground and hence a good short. The bias network (6) for the FET is a little more involved because the threshold voltage is negative. Here a dual power supply is needed.

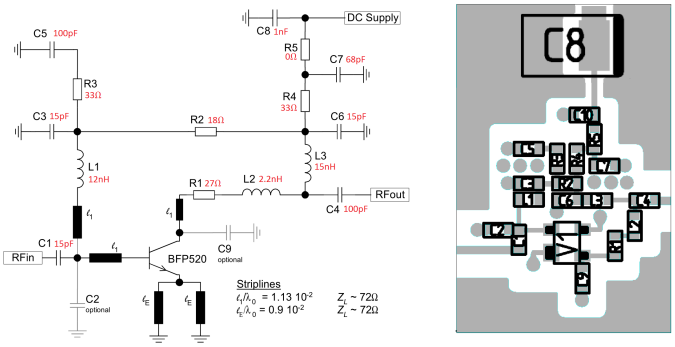


Figure 13. The third example is a 1.9GHz low noise amplifier built around the BFP520.

C. *Example 3:* $1.9GHz$ *low noise amplifier with the BFP520*

The final example is a low noise amplifier designed around the BFP520. The matching is mainly performed with lumped components. The designers use 0402 surface mount components at these high frequencies, resulting in a circuit that is impossible to solder by hand. The small size of the lumped components increases their performance at high frequencies however.

Biasing is done with resistors R_1, R_2 and R_4 to obtain a collector current of 6mA. The resistor R_5 is a 0Ω resistor, which can be replaced by something else if needed. Capacitors C_7 and C_8 decouple the 2V power supply.

The output matching network is built with L_2, L_3, C_6, R_1 and a very small piece of transmission line . The resistor is used in the matching network to improve the stability. To allow even more stabilisation, room is left open for extra capacitors C_2 and C_9, all this because the transistor shows potential instability at 1GHz. The input matching network consists of C_1, L_1, C_3 and R_3. The 100pF capacitors C_4 and C_5 can be considered as shorts at 1.9GHz.

Peculiar in this design is the small amount of emitter feedback added to the transistor. The small pieces of transmission line between the emitter leads and the via to ground will act as inductive feedback.

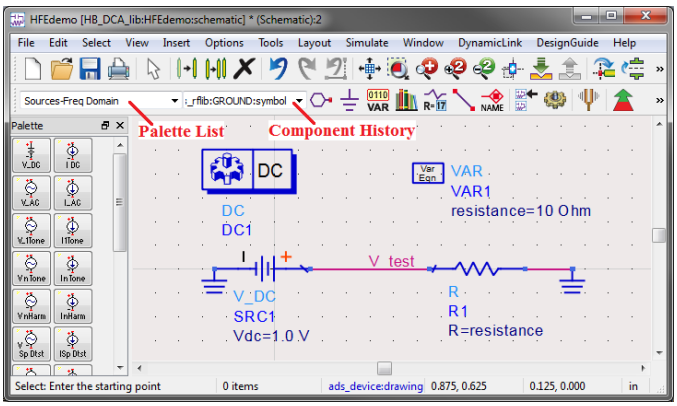


Figure 14. Schematic window in ADS

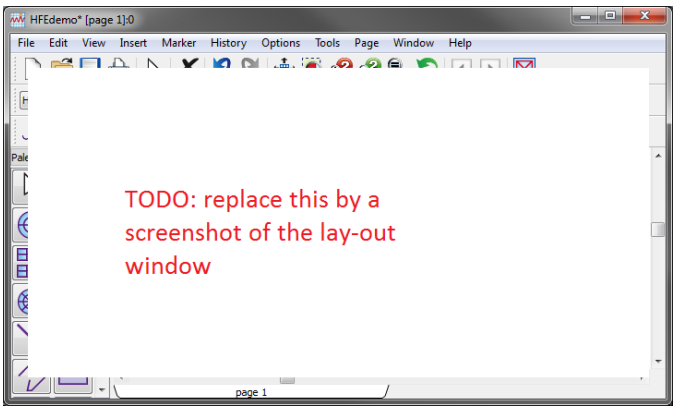


Figure 15. Lay-out window in ADS

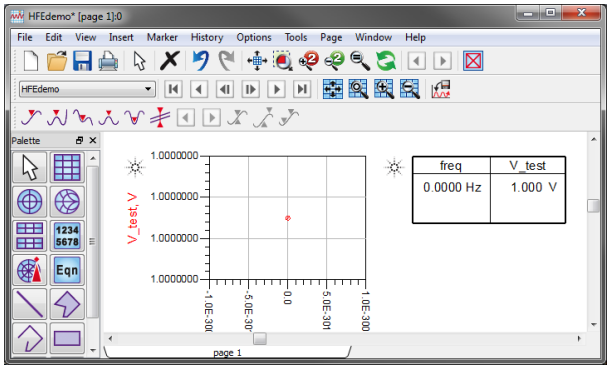


Figure 16. Data display window in ADS

A SMALL INTRODUCTION ON ADS

Advanced Design System (ADS) is electronic design software developed by Keysight[2], an important manufacturer of measurement equipment in the world. ADS is specialised in design for RF and microwave circuits with its built-in electromagnetic simulator, large libraries for components and design guides for most of the circuits encountered in high-frequency circuits. The main competitor for ADS is called Microwave Office, which is developed by National Instruments.

ADS gathers different schematics of a project in a workspace. The workspace is a folder that contains all the files. In a workspace, there are different cells representing the different circuits in a project. Each cell contains different representations of the same design inside of it. Your cells will contain a schematic, a lay-out and possibly a symbol.

The schematic is a schematic representation of your design. It contains the different components and simulation controllers. We provide a short summary of the components you will need during this project below. They can be found in one of the different component palletes or by tying their name in the component history box on top (see Figure 14).

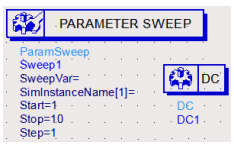
Most of the components have some parameters. You can edit the parameters directly from the schematic window or by double-clicking on the component. Adding units to the values can be done but it is not obliged. A capacitor with value of 5pF will behave the same as one with a value of 5e-12. It's possible to define variables in your schematic and to perform calculations in the schematic window.

When you are satisfied with a design, you can generate its lay-out, or generate a symbol to use the design in other cells in the workspace.

Lay-out window: You can automatically generate the lay-out of a circuit by pressing *Layout→Generate/Update*. The generated lay-out will then appear as an extra file in the cell and the lay-out window will open (Figure 15). Each component of the schematic is represented by its lay-out object. If a component has no lay-out, a large box will appear. You can add extra components from the component palette on the left, or draw extra shapes using the *insert* menu on top. The layer on which you are drawing is controlled by the drop-down menu on the top right.

Simulation data and data displays: When you run a simulation, all simulations specified in the schematic are run sequentially. The simulation results are saved into a dataset (.ds file), which is located in the folder of the workspace. The simulation data can be visualised in a data display (.dds file). A blank data display is generated automatically when you run a simulation in a schematic for the first time. In that data display you can add plots to visualise your simulation data (Figure 16). You choose the type of plot on the left and place it on the data display. You will then be prompted to choose the data that has to be shown in the plot.

LIST OF COMPONENTS YOU WILL NEED IN ADS

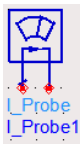


DC simulation component. If you add this to your schematic, a DC simulation will be performed. You can inspect the result in a data display, or annotate the DC solution by clicking *Simulate → Annotate DC solution.*

With a **ParamSweep**, you can sweep a variable in the schematic. The name of the variable is given

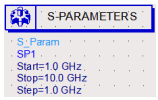
[2]previously called Agilent, but they changed name in 2014. Originally, this company was part of Hewlett-Packard. You can still notice artefacts of this in history ADS. The underlying simulator is called hpeesofsim, because HP acquired the eesof simulator in 1993

in the *SweepVar* field, The simulation component that has to be swept is given by the *SimInstanceName*. The range over which the variable has to be swept is given by the *Start*, *Step* and *Stop* variables.

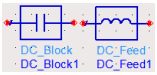


With an **I_probe**, you can measure a current in the schematic. The result will appear in the simulation variable as *I_probe1.i*. **V_DC** and **I_DC** are the ideal DC voltage and current sources respectively.

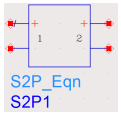
The **S_param** block is the simulation controller for an S-parameter simulation. You can set the frequencies for which the S-parameters are calculated in this block. When you press Simulate, the block looks for *Term* components and gives the S-parameters between those blocks. If 2 *Term* blocks are present, a 2x2 S-matrix is returned in the results.



Ports used by the S-parameter simulation. You can set the reference impedance and the number of the port as parameters to the term. Keep in mind that this block will act as a 50Ω resistor for the DC simulation, so make sure that your biasing cannot flow into the port by using a DC_block component.

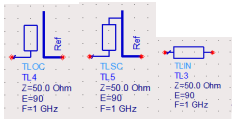


DC_Block and **DC_Feed** are the ideal capacitor and ideal coils. The ideal capacitor blocks DC, but lets all AC signals pass through. The ideal coil blocks all AC signals, but lets the DC through.

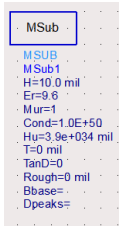


You can use the **S2P_Eqn** block to replace the transistor, once you know its S-parameters. Working with this block allows to make the transistor unilateral by setting the reverse gain S_{12} to 0.

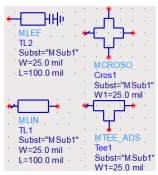
TLIN represents the Ideal transmission line, which is a delay without losses. You can set the electrical length E at the specified frequency F. An electrical length of 360 degrees corresponds to a line of a full wavelength.



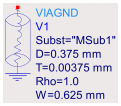
TLSC and **TLOC** are ideal stubs, terminated in an open and short circuit respectively. Both can be used as a stub in the matching network. Keep in mind that TLSC component is a short to ground at DC, this might mess with the biasing.



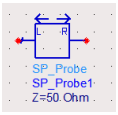
MSUB describes the substrate on which the transmission lines are placed. The parameters that have to be filled in here can be found in the PCB datasheet. H is the thickness of the substrate, Er is the relative permittivity of the dielectric, $Cond$ is the conductivity of the metal used for the transmission lines, T is the metal thickness and $TanD$ is the loss tangent of the dielectric.



MLIN is the basic microstrip transmission line. You can set the width and the length. **MLEF** is the Open-circuited stub. Don't be fooled, the capacitor at the end is not a capacitor, but a representation of the fringing fields that are present if you make an open circuit. **MTEE** and **MCROSO** can be used to connect 3 and 4 lines together. The dimensions indicate the width of the connections.

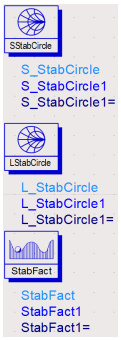


The **VIAGND** component represents a ground connection made by connecting the top metal of the pcb to the ground plane on the bottom with a VIA. On high frequencies, these connections introduce significant inductance, so their effect should be taken into account. The component uses the properties of a PCB by referring to the substrate in its *Subst* parameter. width of the hole in the via is given in the *D* parameter, while the metallisation width is provided in *T*. The *W* parameter is used to specify the width of the metal island around the VIA itself.



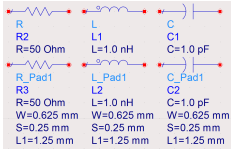
The **SP_Probe** component allows to determine the S-parameters seen left and right of the probe. This is a very usefull block if you want to see, for example, which reflection a bias network presents to your circuit. When the circuit is matched, an Sp_Probe placed at the transistor should see complex conjugate reflection factors left and right.

The SP_Probe adds *L.S(1,1)* and *R.S(1,1)* to the simulation results. They represent the reflection factor seen left and right respectively. If you have multiple SP_Probes in your circuit, the name of the probe will be added in front of the variable in the simulation results. For the probe shown here the variable will be called *SP_Probe1.L.S(1,1)*.



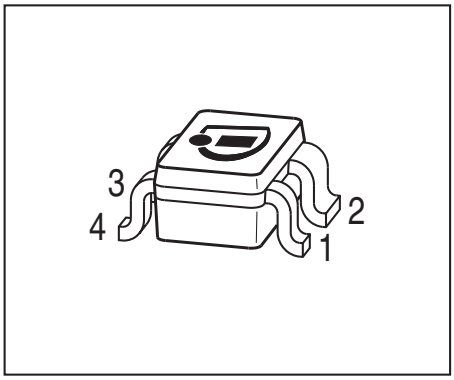
ADS can calculate the stability circles for a given design automatically using the **S_StabCircle** and **L_StabCircle** components. When an S-parameter simulation is present, the resulting S-matrix is used to calculate the circles, so the stability circles are given for the whole circuit between the ports. If you want the stability circles for the transistor alone, you have to add the blocks to a schematic where the transistor is present without matching network. For each simulation frequency, a stability circle is calculated, so when a frequency sweep is performed, the results can become confusing.

The stability Factor can be calculated automatically by placing the **StabFact** component in the schematic window. The stability factor is a single number for each frequency, so it is easier to use in frequency sweeps.



Finally, we have the passives, **R**, **L** and **C** for resistors, inductors and capacitors. The default passives have no lay-out attached to them, so when the lay-out is generated, large gaps occur at their location. To be able to specify the physical dimensions of the surface-mount components, you should use **R_Pad1**, **L_Pad1** and **C_Pad1**. These components have a lay-out on which the component can be soldered.

Low Noise Silicon Bipolar RF Transistor



- Low noise amplifier designed for low voltage applications, ideal for 1.2 V or 1.8 V supply voltage. Supports V_{cc} = 2.9 V with enough external collector resistance.
- High gain and low noise at high frequencies due to high transit frequency f_T = 45 GHz
- Common e.g. in cordless phones and satellite receivers
- Easy to use Pb-free (RoHS compliant) and halogen free industry standard package with visible leads
- Qualification report according to AEC-Q101 available

RoHS HAL

ESD (**E**lectro**s**tatic **d**ischarge) sensitive device, observe handling precaution!

Type	Marking	Pin Configuration						Package
BFP520	APs	1=B	2=E	3=C	4=E	-	-	SOT343

Maximum Ratings at T_A = 25 °C, unless otherwise specified

Parameter	Symbol	Value	Unit
Collector-emitter voltage	V_{CEO}		V
T_A = 25 °C		2.5	
T_A = -55 °C		2.4	
Collector-emitter voltage	V_{CES}	10	
Collector-base voltage	V_{CBO}	10	
Emitter-base voltage	V_{EBO}	1	
Collector current	I_C	50	mA
Base current	I_B	5	
Total power dissipation[1)] $T_S \leq 105$ °C	P_{tot}	125	mW
Junction temperature	T_J	150	°C
Storage temperature	T_{Stg}	-55 ... 150	

[1] T_S is measured on the emitter lead at the soldering point to pcb

Thermal Resistance

Parameter	Symbol	Value	Unit
Junction - soldering point[1)]	R_{thJS}	450	K/W

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
DC Characteristics					
Collector-emitter breakdown voltage I_C = 1 mA, I_B = 0	$V_{(BR)CEO}$	2.5	3	3.5	V
Collector-emitter cutoff current	I_{CES}				nA
V_{CE} = 2 V, V_{BE} = 0		-	1	30	
V_{CE} = 10 V, V_{BE} = 0		-	-	1000	
Collector-base cutoff current V_{CB} = 2 V, I_E = 0	I_{CBO}	-	-	30	
Emitter-base cutoff current V_{EB} = 0.5 V, I_C = 0	I_{EBO}	-	100	3000	
DC current gain I_C = 20 mA, V_{CE} = 2 V, pulse measured	h_{FE}	70	110	170	-

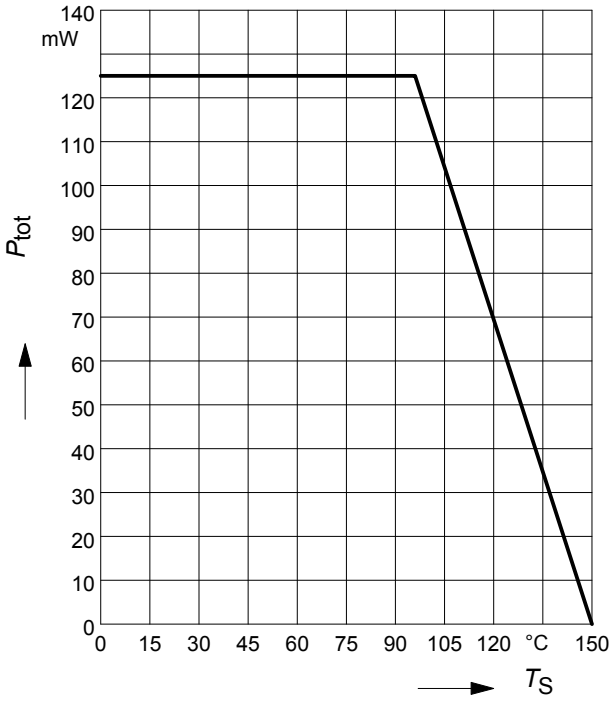
[1]For the definition of R_{thJS} please refer to Application Note AN077 (Thermal Resistance Calculation)

Electrical Characteristics at T_A = 25°C, unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
AC Characteristics (verified by random sampling)					
Transition frequency I_C = 30 mA, V_{CE} = 2 V, f = 2 GHz	f_T	32	45	-	GHz
Collector-base capacitance V_{CB} = 2 V, f = 1 MHz, V_{BE} = 0 , emitter grounded	C_{cb}	-	0.07	0.13	pF
Collector emitter capacitance V_{CE} = 2 V, f = 1 MHz, V_{BE} = 0 , base grounded	C_{ce}	-	0.3	-	
Emitter-base capacitance V_{EB} = 0.5 V, f = 1 MHz, V_{CB} = 0 , collector grounded	C_{eb}	-	0.33	-	
Minimum noise figure I_C = 2 mA, V_{CE} = 2 V, Z_S = Z_{Sopt} , f = 1.8 GHz	NF_{min}	-	0.95	-	dB
Power gain, maximum stable[1)] I_C = 20 mA, V_{CE} = 2 V, Z_S = Z_{Sopt}, Z_L = Z_{Lopt} , f = 1.8 GHz	G_{ms}	-	24	-	dB
Insertion power gain V_{CE} = 2 V, I_C = 20 mA, f = 1.8 GHz, Z_S = Z_L = 50 Ω	$\lvert S_{21}\rvert^2$	-	21.5	-	
Third order intercept point at output V_{CE} = 2 V, I_C = 20 mA, f = 1.8 GHz, Z_S = Z_{Sopt}, Z_L = Z_{Lopt} V_{CE} = 2 V, I_C = 7 mA, f = 1.8 GHz, Z_S = Z_{Sopt}, Z_L = Z_{Lopt}	IP_3	 - -	 25 17	 - -	dBm
1dB compression point at output I_C = 20 mA, V_{CE} = 2 V, Z_S = Z_{Sopt}, Z_L = Z_{Lopt}, f = 1.8 GHz I_C = 7 mA, V_{CE} = 2 V, Z_S = Z_{Sopt}, Z_L = Z_{Lopt}, f = 1.8 GHz	P_{-1dB}	 - -	 12 5	 - -	

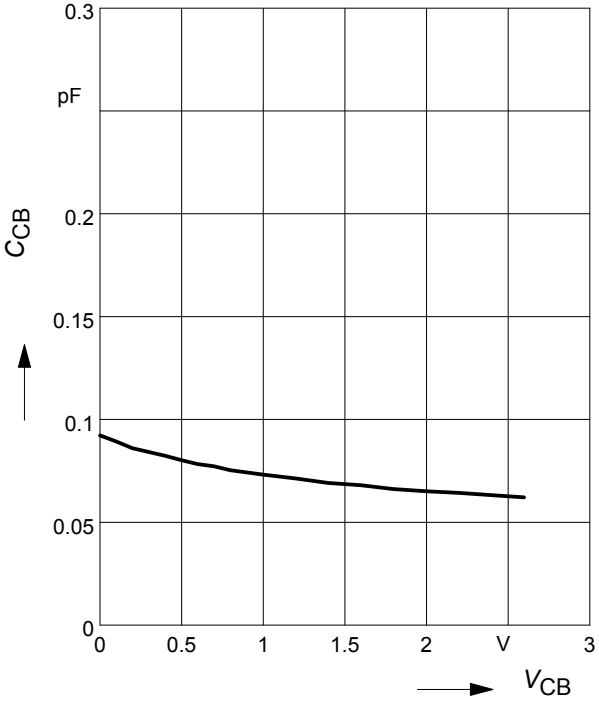
[1] $G_{ms} = |S_{21} / S_{12}|$

Total power dissipation $P_{tot} = f(T_S)$



Collector-base capacitance $C_{cb} = f(V_{CB})$

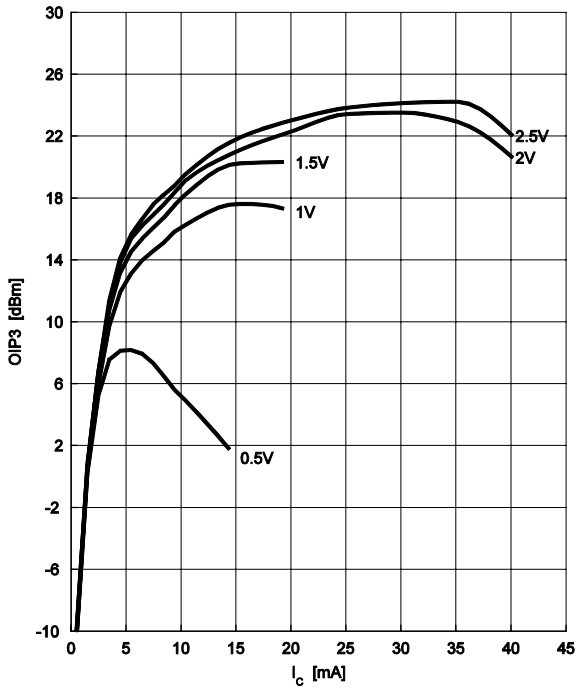
f = 1MHz



Third order Intercept Point $IP_3 = f(I_C)$

(Output, $Z_S = Z_L = 50\ \Omega$)

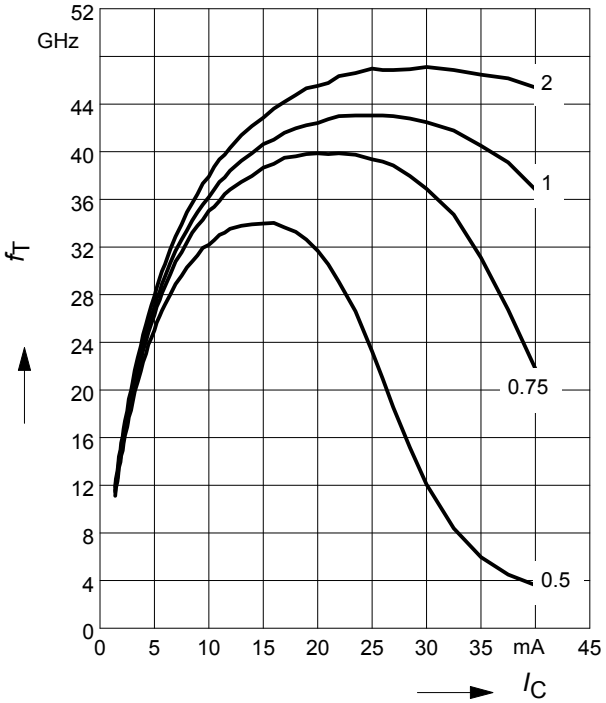
V_{CE} = parameter, f = 900 MHz



Transition frequency $f_T = f(I_C)$

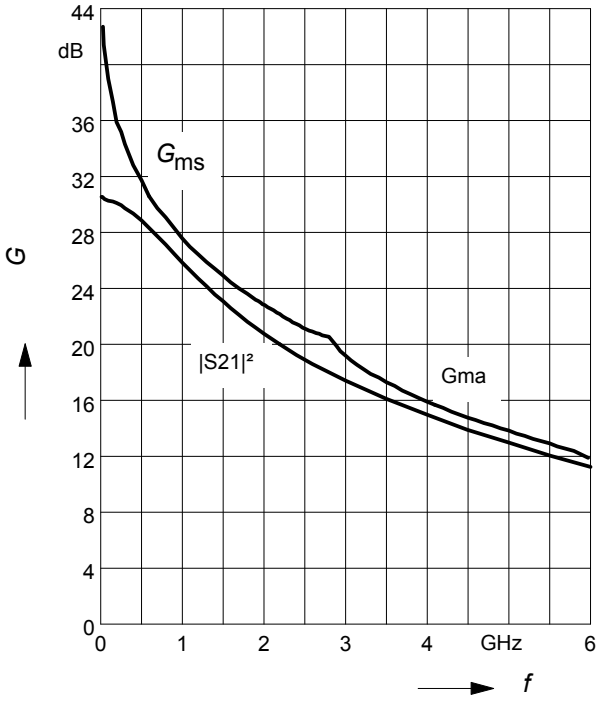
f = 2 GHz

V_{CE} = parameter in V



Power gain G_{ma}, G_{ms}, $|S_{21}|^2 = f(f)$

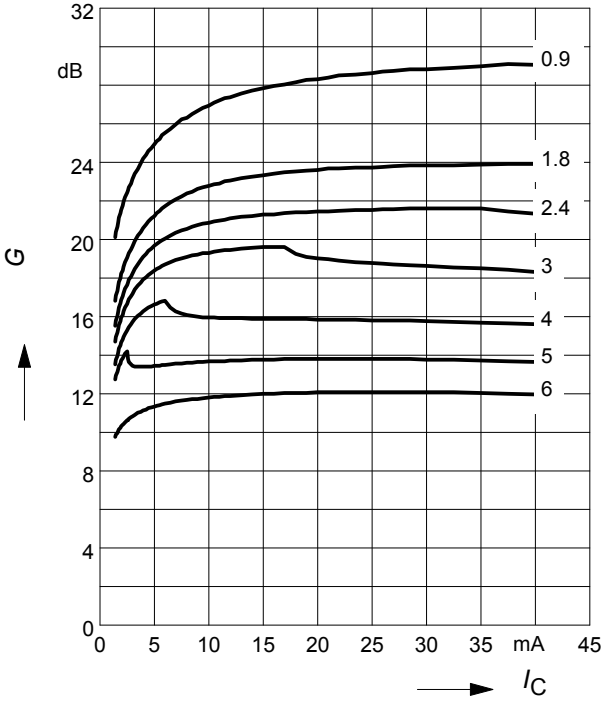
V_{CE} = 2 V, I_C = 20 mA



Power gain G_{ma}, G_{ms} = $f(I_C)$

V_{CE} = 2V

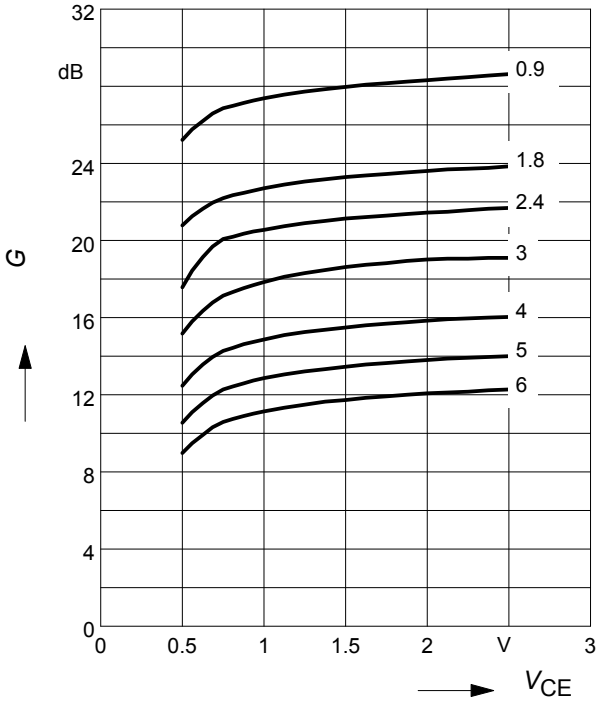
f = parameter in GHz



Power gain G_{ma}, G_{ms} = $f(V_{CE})$

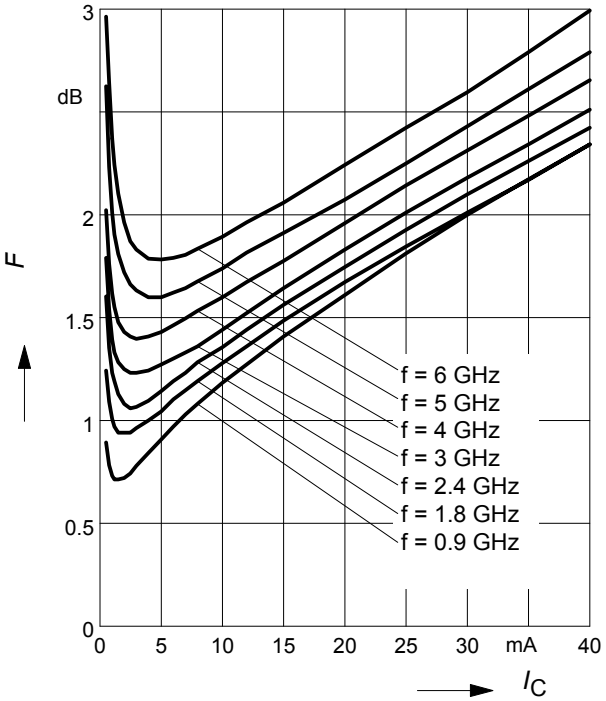
I_C = 20 mA

f = parameter in GHz



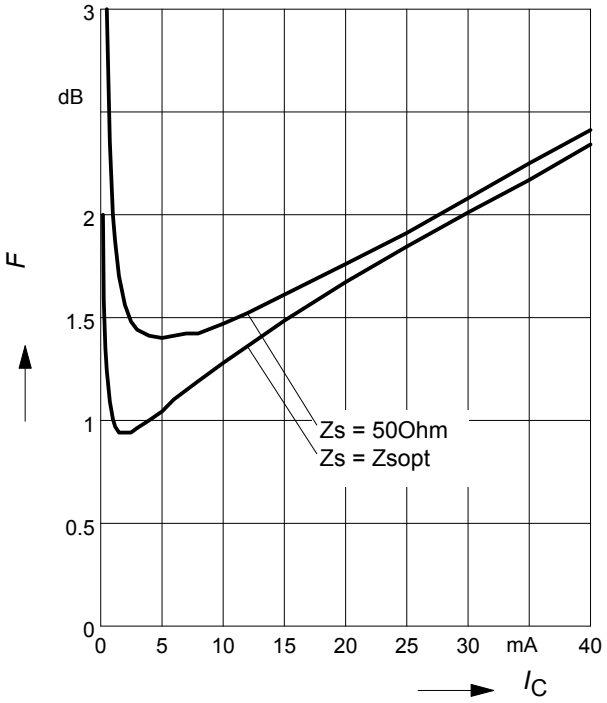
Minimum noise figure NF_{min} = $f(I_C)$

V_{CE} = 2 V, Z_S = Z_{Sopt}



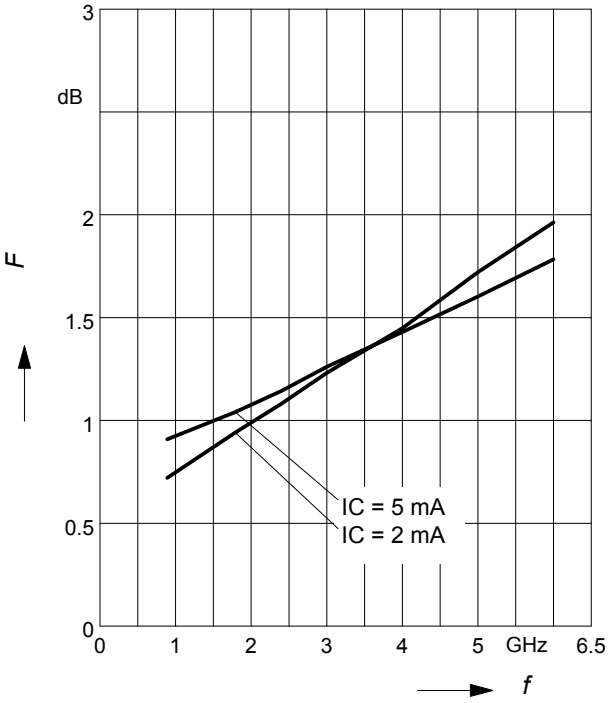
Noise figure $F = f(I_C)$

V_{CE} = 2 V, f = 1.8 GHz



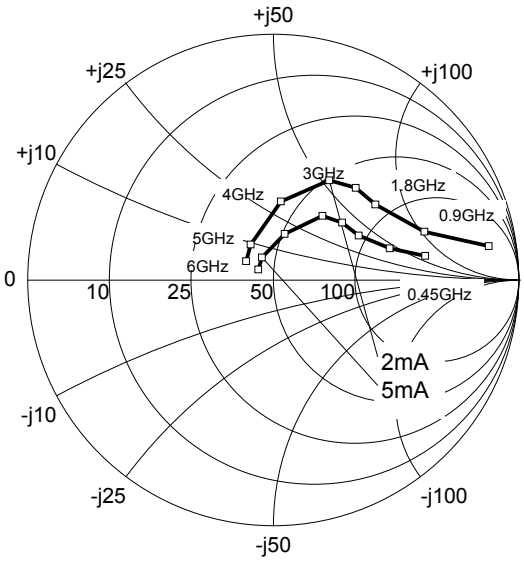
Minimum noise figure $NF_{min} = f(f)$

V_{CE} = 2 V, $Z_S = Z_{Sopt}$

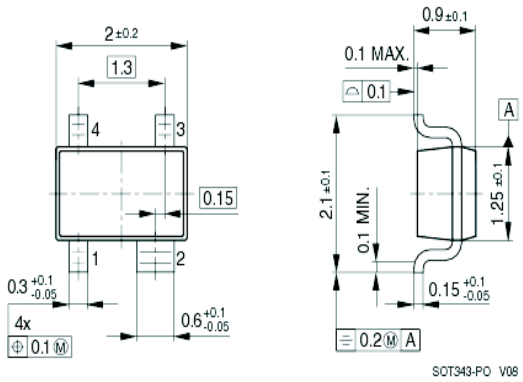


Source impedance for min. noise figure vs. frequency

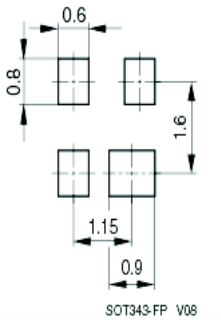
V_{CE} = 2 V, I_C = 2 mA / 5 mA



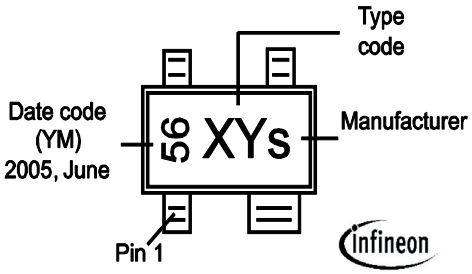
Package Outline



Foot Print

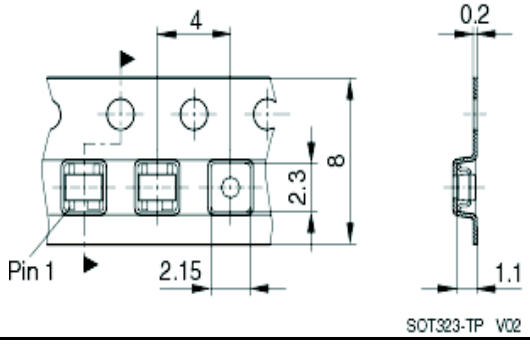


Marking Layout (Example)



Standard Packing

Reel Ø180 mm = 3.000 Pieces/Reel
Reel Ø330 mm = 10.000 Pieces/Reel



Package SOT 343.vsd

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ROGERS CORPORATION

Advanced Circuit Materials

Data Sheet
1.4360 Data Sheet

RO4360™ High Frequency Laminates

Features:	**Benefits:**
RO4000® thermoset resin system specially formulated to meet 6.15 DK	• Ease of fabrication / processes similar to FR-4 • RO4000 material repeatability • Low Loss • High thermal conductivity • Lower total PCB cost solution than competing PTFE products
Low Z-axis CTE / High Tg	• Design flexibility • Plated through-hole reliability • Automated assembly compatible
Environmentally friendly	• Lead free process compatible
Regional finished goods inventory	• Short lead times / quick inventory turns • Efficient supply chain
Typical Applications:	
• Power Amplifiers for Cell Phone Base Stations	
• Patch Antenna	

RO4360™ laminates are 6.15 DK, low loss, glass-reinforced, ceramic-filled thermoset materials that provide the ideal balance of performance and processing ease. RO4360 laminate extends Rogers' portfolio of high performance materials by providing customers with a product that is lead-free process capable and offers better rigidity for improved processability and multi-layer board construction, while reducing material and fabrication costs.

RO4360 laminates process similar to FR-4 and are automated assembly compatible. They have a low Z-axis CTE for design flexibility and have the same high Tg as all of the RO4000 product line. RO4360 laminates can be paired with RO4400™ prepreg and lower-DK RO4000 laminate in multilayer designs.

RO4360 laminates, with a DK of 6.15, allow designers to reduce circuit dimensions in applications where size and cost are critical. They are the best value choice for engineers working on designs including power amplifiers, patch antennas, ground-based radar, and other general RF applications.

Typical Values				RO4360™ High Frequency Laminates	
Property	**Typical Value [1]**	**Direction**	**Units**	**Condition**	**Test Method**
Dielectric Constant, ε_r (Process Specification)	6.15 ± 0.15	Z		10 GHz/23°C	IPC-TM-650 2.5.5.5 [2] Clamped Stripline
				2.5 GHz/23°C	
Dielectric Constant, ε_r (Recommend for use in circuit design)	6.15	Z		FSR/23°C	IPC-TM-650 2.5.5.6 Full Sheet Resonance
Dissipation Factor	0.0038	Z		10 GHz/23°C	IPC-TM-650, 2.5.5.5
	0.003			2 GHz/23°C	
Thermal Conductivity	0.8		W/m/K		IPC-TM-650 2.5.2.1
Volume Resistivity	1.30E+12		MΩ•cm	COND A	IPC-TM-650, 2.5.17.1
Surface Resistivity	3.11E+11		MΩ	COND A	IPC-TM-650, 2.5.17.1
Electrical Strength	23.8 (605)	Z	KV/mm (V/mil)		IPC-TM-650, 2.5.6.2
Tensile Modulus	10000 (1500)		MPa (kpsi)	RT	ASTM D638
Tensile Strength	97 (14)		MPa (kpsi)	RT	ASTM D638
Flexural Strength	190 (28)		MPa (kpsi)		IPC-TM-650, 2.4.4
Dimensional Stability	0.0 0.1	X Y	mm/m (mils/inch)		IPC-TM-650, 2.4.39A
Lead-Free Process Compatible	Yes				
Coefficient of Thermal Expansion	16.6	X	ppm/°C		IPC-TM-650, 2.1.41
	14.6	Y			
	30	Z			
Tg	>280		°C TMA		ASTM D3850
Td	>350		°C TGA		ASTM D3850
T288	>30	Z	min	30 min / 125°C Prebake	IPC-TM-650 2.4.24.1
Moisture Absorption	0.13		%		IPC-TM-650 2.6.2.1 ASTM D570
Thermal Coefficient of ε_r	-120	Z	ppm/°C	-100°C to 250°C	IPC-TM-650, 2.5.5.5
Density	2.16		gm/cm3		ASTM D792
Copper Peel Strength	5.2		pli (N/mm)		IPC-TM-650 2.4.8
Flammability	94V-0 (Pending)				UL94 File QMTS2.E102763

[1] Typical values are a representation of an average value for the population of the property. For specification values contact Rogers Corporation.
(2) Clamped stripline method can potentially lower the actual dielectric constant due to presence of airgap. Dielectric constant in practice may be higher than the value listed.

Prolonged exposure in an oxidative environment may cause changes to the dielectric properties of hydrocarbon based materials. The rate of change increases at higher temperatures and is highly dependent on the circuit design. Although Rogers' high frequency materials have been used successfully in in-numerable applications and reports of oxidation resulting in performance problems are extremely rare, Rogers recommends that the customer evaluate each material and design combination to determine fitness for use over the entire life of the end product.

Standard Thickness	Standard Panel Size:	Standard Copper Cladding
0.008" (0.203mm), 0.012" (0.305mm) 0.016"(0.406mm), 0.020" (0.508mm) 0.032" (0.813mm), 0.060" (1.524mm)	12" X 18" (305 X457 mm) 24" X 18" (610 X 457 mm) 48" X 36" (1.224 m X 915 mm)	½ oz. (18µm), 1 oz. (35µm) and 2 oz. (70µm) electrodeposited copper foil

The information in this data sheet is intended to assist you in designing with Rogers' circuit material laminates. It is not intended to and does not create any warranties express or implied, including any warranty of merchantability or fitness for a particular purpose or that the results shown on this data sheet will be achieved by a user for a particular purpose. The user should determine the suitability of Rogers' circuit material laminates for each application.

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Issued 08/2009 0878-0809 **Publication #92-143**

Capacitor data sheet

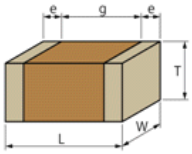
GQM2195C2A5R6CB01#

" # " indicates a package specification code.

Recommended | Flow OK | Reflow OK | Complies with RoHS | HIQ

< List of part numbers with package codes >
GQM2195C2A5R6CB01D , GQM2195C2A5R6CB01J

Shape



L size	2.0 ±0.1mm
W size	1.25 ±0.1mm
T size	0.85 ±0.1mm
External terminal width e	0.2 to 0.7mm
Distance between external terminals g	0.7mm min.
Size code in inch(mm)	0805 (2012)

References

Packaging	Specifications	Minimum quantity
D	φ180mm Paper taping	4000
J	φ330mm Paper taping	10000

Mass (typ.)	
1 piece	9.5mg
φ180mm Reel	152g

Specifications

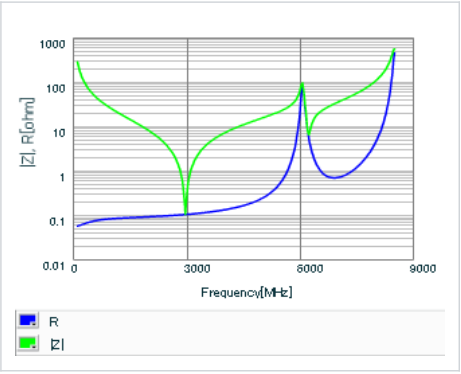
Capacitance	5.6pF ±0.25pF
Rated voltage	100Vdc
Temperature characteristics (complied standard)	C0G(EIA)
Temperature coefficient	0±30ppm/℃
Temperature range of temperature characteristics	25 to 125℃
Operating temperature range	-55 to 125℃

Murata Manufacturing Co., Ltd. URL : http://www.murata.co.jp/

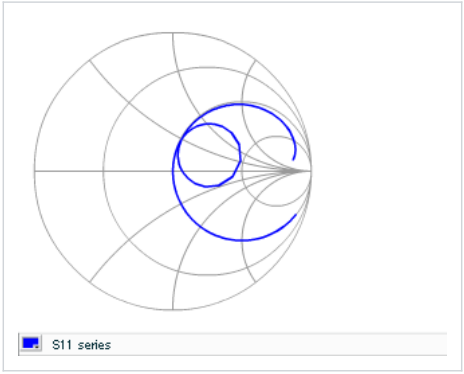
Last updated: 2014/02/19

Chart of characteristic data (The charts below may show another part number which shares its characteristics.)

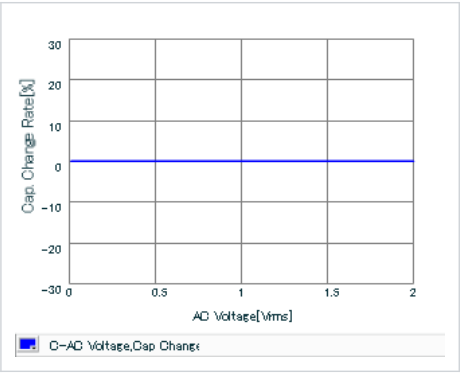
- Frequency characteristics (ESR, Impedance)



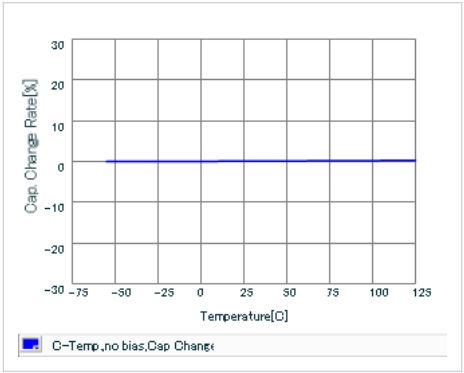
- S parameter (Smith chart S11)



- AC voltage characteristics



- Capacitance - temperature characteristics



muRata Murata Manufacturing Co., Ltd.
Last updated: 2014/02/19

SMA - 50 Ohm Connectors

End Launch Connectors - A Johnson Components™ Original

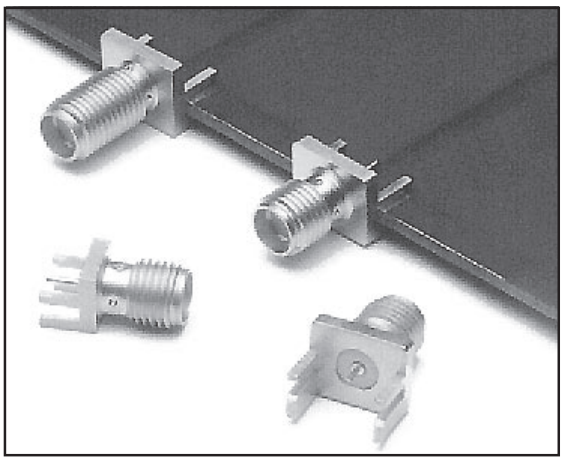
EMERSON Network Power

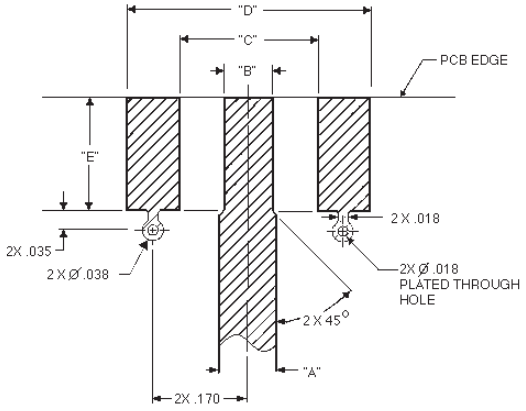
INCHES (MILLIMETERS)
CUSTOMER DRAWINGS AVAILABLE UPON REQUEST

The **End Launch** connector is attached to the circuit board by inserting the board edge between the legs and soldering the legs and center conductor to pads on the board. For optimum high frequency performance, the connector to circuit board transition must be adjusted for low VSWR. To compensate for the transition from coax to microstrip, trace widths “A” and “B” must be adjusted based on circuit board thickness. When properly adjusted, this technique yields a low VSWR over a wide bandwidth.

The tabulated dimensions "A", "B", "C", "D", and "E" were determined experimentally to achieve low VSWR (typically less than 1.5 up to 18 GHz). The circuit board used for these tests was double-sided FR 4 with 1 oz. copper on both sides. The copper was left on the bottom of the board to create a ground plane for the 50 Ohm microstrip structure. While not all inclusive, these dimensions are given as reference information for selected **SMA End Launch** connectors. Further adjustments may be necessary depending upon the application. All dimensions are in inches.

Tabulated Dimensions "A", "B", "C" and "D" are symmetrical about the center line





Part Number	Base Width	Board Thick	"A"	"B"	"C"	"D"	"E"
142-0701-801/806	.375	.062	.103	.090	.250	.440	.200
142-0701-851/861	.375	.062	.103	.090	.250	.440	.200
142-0701-871/876	.375	.062	.103	.090	.250	.440	.200
142-0711-821/826	.250	.062	.103	.070	.170	.380	.165
142-0711-871/876	.375	.047	.083	.075	.250	.440	.200
142-0711-881/886	.375	.047	.083	.075	.250	.440	.200
142-0701-881/886	.375	.031	.050	.045	.250	.440	.200

Surface Mount Versions Available!

SMA End Launch Specifications

ELECTRICAL RATINGS
Impedance: 50 Ohms
Frequency Range: 0-18 GHz
VSWR: Dependent upon application
Working Voltage (VRMS max.): 335 @ Sea Level, 85 @ 70K Feet
Dielectric Withstanding Voltage (VRMS min. at sea level): 1000
Corona Level (Volts min. at 70,000 feet): 250
Insulation Resistance: 5000 megohms min
Contact Resistance (milliohms max.): 3.0 Initial, 4.0 after environmental
RF High Potential Withstanding Voltage (VRMS min. tested at 4 and 7 MHz): 670

MECHANICAL RATINGS
Engagement Design: MIL-C-39012, Series SMA
Engagement/Disengagement Force: 2 inch-pounds max.
Mating Torque: 7 to 10 inch-pounds
Coupling Proof Torque: 15 inch-pounds min.
Coupling Nut Retention: 60 pounds min.
Contact Retention Force: 6 lbs min. axial force, 4 inch-ounce min. torque
Durability: 500 cycles min.

ENVIRONMENTAL RATINGS:
(Meets or exceeds the applicable paragraph of MIL-C-39012)
Temperature Range: -65° to + 165° C
Thermal Shock: MIL-STD-202, Method 107, Condition B
Corrosion: MIL-STD-202, Method 101, Condition B
Shock: MIL-STD-303, Method 213, Condition I
Vibration: MIL-STD-202, Method 204, Condition D
Moisture Resistance: MIL-STD-202, Method 106

MATERIAL SPECIFICATIONS
Bodies: Brass per QQ-B-626, gold plated* per MIL-G-45204 .00001” min. or nickel plated per QQ-N-290
Contacts: Male - brass per QQ-B-626, gold plated per MIL-G-45204 .00003” min.
Female - beryllium copper per QQ-C-530, gold plated per MIL-G-45204 .00003” min.
Nut Retention Spring: Beryllium copper per QQ-C-533. Unplated
Insulators: PTFE fluorocarbon per ASTM D 1710 and ASTM D 1457
Mounting Hardware: Brass per QQ-B-626 or QQ-B-613, gold plated per MIL-G-45204 .00001” min. or nickel plated per QQ-N-290

*All gold plated parts include a .00005” min. nickel underplate barrier layer.

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